

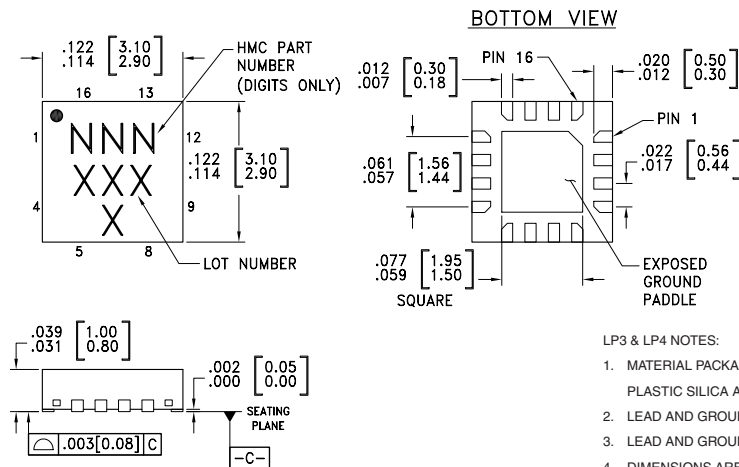
PCB DESIGN AND ASSEMBLY FOR QFN (LPCC) PACKAGES

Introduction

The need for low-cost surface mount plastic packages that operate to high frequency with low package thermal resistance has led to the development of Quad Flatpack No-Lead (QFN) packages. The industry standard description for these packages is JEDEC MO-220 or "Thermally enhanced plastic very thin and very fine pitch quad flat no lead package (QFN)". Hittite Microwave Corporation offers standard products in QFN packages operating at frequencies up to 16 GHz. To successfully integrate these new packages into a system design, proper PCB layout, handling and assembly guidelines must be followed.

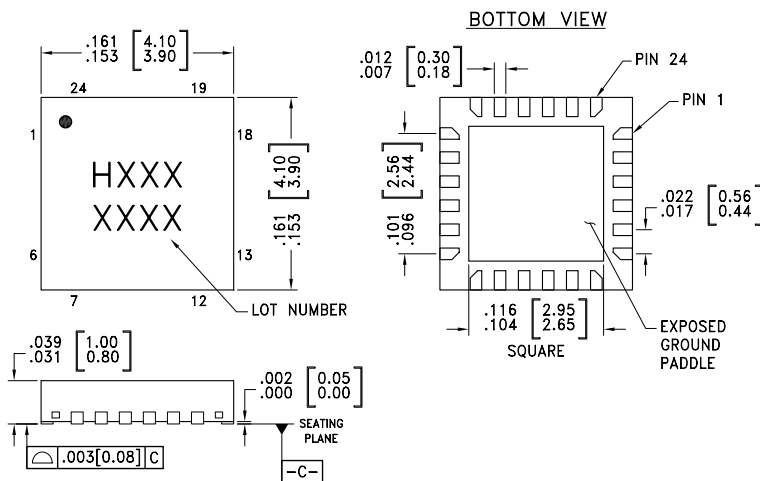
General Description of QFN (LPCC) Packages

Hittite standard products that make use of QFN packages carry the simple suffix "LP3" or "LP4", representing leadless packages that are 3x3mm (figure 1a) or 4x4mm (figure 1b) in size. These packages typically contain 16 and 24 I/Os respectively and have exposed metal on the underside of the package that must be attached to both an RF ground plane and a proper thermal path.



LP3 & LP4 NOTES:

1. MATERIAL PACKAGE BODY: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
3. LEAD AND GROUND PADDLE PLATING: Sn/Pb SOLDER
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
6. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.



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PCB Solder Mask and Land Pattern Design

Due to the dense land pattern and exposed metal base of the QFN package, the PCB land pattern geometry is critical. The application of a solder mask is required, and must be applied to the PCB between the land pads and the ground pad. A minimum solder mask web of 0.010 inches [0.25 mm] between the land pads and the ground pad should be used in order to prevent shorting. Unless solid-filled vias are used, solder stop must also be applied to the backside of the PCB under the LP3/LP4 to prevent depletion (or wicking) of the solder paste from the device ground pad through the plated via holes during the reflow process.

The land pattern and solder mask pattern for the LP3 and LP4 packages are shown with their proper alignment in figure 2a and 2b respectively.

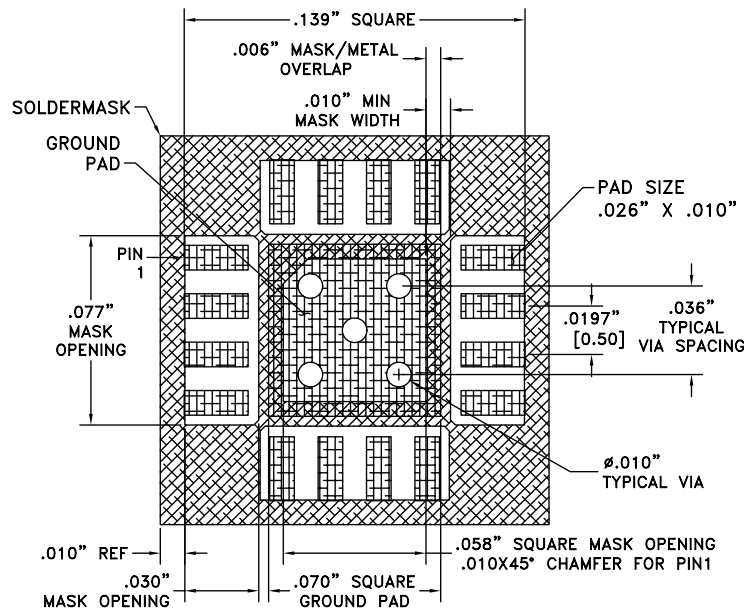


Figure 2a – LP3 solder mask and land pattern

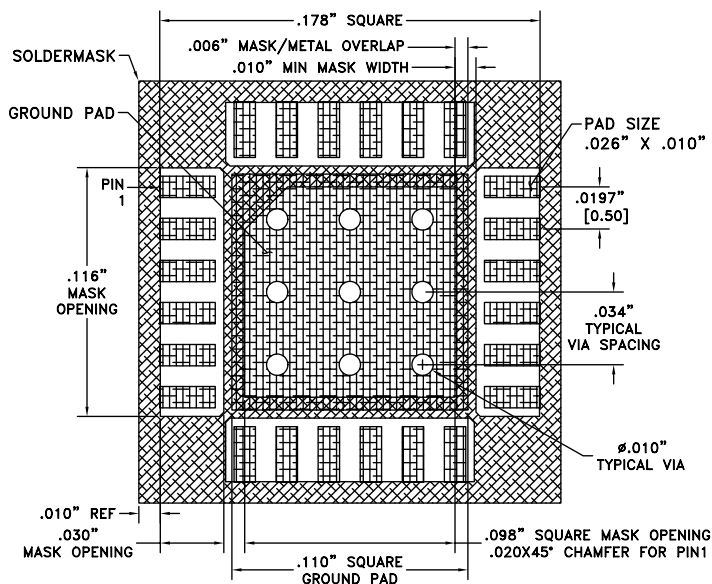


Figure 2b – LP4 solder mask and land pattern

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Solder Paste Application

Hand soldering of LP3 and LP4 packages is not recommended due to the fine pitch of the package leads and the inability to properly attach the exposed metal base to the PCB. Furthermore, the use of conductive epoxy is not recommended since these epoxies will bleed, causing shorts between lands and they do not have sufficient thermal properties.

Solder paste must be used to attach QFN packages to the PCB. For proper solder thickness and alignment, the solder paste must be applied to the PCB using a stencil printer. The volume of solder paste dispensed via screen-printing will be dependent on the stencil opening and stencil thickness. A recommended stencil pattern for the LP3 and LP4 package to be used with SN63 solder paste is shown in figure 3a and 3b respectively. Stencil alignment to the PCB land pattern should be to within +/-1 mil to prevent formation of solder balls between the lands during the reflow process. A PCB with properly screened solder paste is shown in Figure 4.

Component Placement

Hand placement of the QFN package is extremely difficult and is not recommended. Therefore a pick-and-place machine with a microscope is recommended for the component placement operation. Careful device placement and minimal pressure will prevent solder paste smearing. To minimize solder paste smearing, the base of the LPCC package should be brought to a height of 3-4 mils above the surface of the PCB. This will result in the LPCC package being pressed 1-2 mils into the solder paste.

Reflow Solder Process

The soldering process is usually accomplished in a reflow oven but may also use a vapor phase process. Prior to reflowing the device, temperature profiles should be measured using the same mass as the actual assemblies. The thermocouple should be moved to various positions on the board to account for edge and corner effects and varying component masses. The final profile should be determined by mounting the thermocouple to the PCB at the location of the device. Follow solder paste and oven vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temperature to avoid damage due to thermal shock. Allow enough time between reaching pre-heat temperature and reflow for the solvent in the paste to evaporate and the flux to completely activate. Reflow must then occur prior to the flux being completely driven off. To help prevent the flux from being driven off, a steady ramp is preferred to the traditional soak. This profile is also preferred for lead-free soldering. The duration of peak reflow temperature should not exceed 15 seconds. QFN Packages have

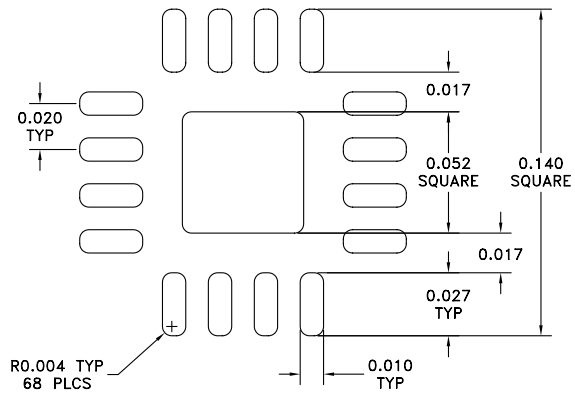


Figure 3a – LP3 solder paste stencil

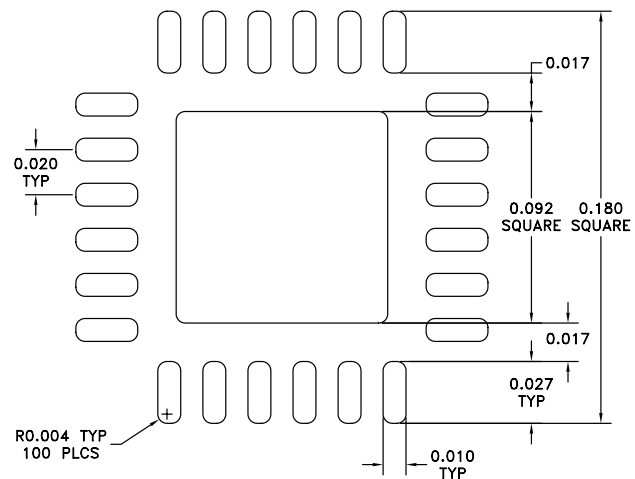


Figure 3b – LP4 solder paste stencil

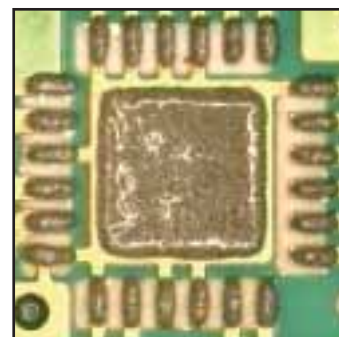


Figure 4 – PCB with properly screen solder paste

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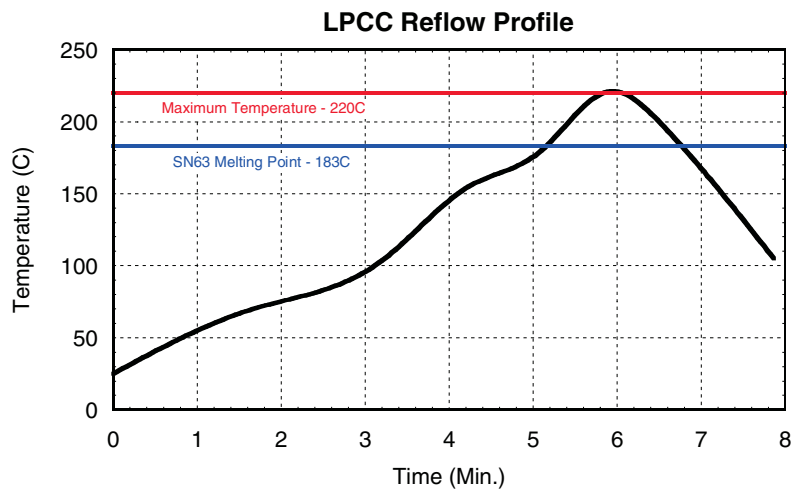


Figure 5 – Typical LPCC reflow profile

been qualified to withstand a peak temperature of 235°C for 15 seconds. Verify that the profile will not expose the device to temperatures in excess of 235°C. A typical reflow profile for the QFN package is shown in Figure 5.

Reworking

In cases where the QFN package must be removed from the PCB and replaced, special tools and procedures are needed. In order to heat the QFN package sufficiently to remove it without reflowing the solder of nearby components, a hot air workstation is recommended with an appropriate tool that limits the exposure of adjacent components to the hot air flow. If the part being removed will be reused, make sure not to exceed the 235°C maximum temperature of the QFN package.

Once the package has been sufficiently heated and the solder has melted, the QFN package should be removed with tweezers. The PCB and the bottom of the QFN package must then be thoroughly cleaned and all solder and flux removed. Solder wick is usually sufficient to remove the solder from the surface of the board and bottom of the QFN package.

Application of the solder paste must meet the criteria previously discussed. This can be accomplished using a solder paste dispenser, although extreme care must be taken to apply the correct amount of paste in the proper locations. A more reliable method is to use a miniature stencil that can be applied directly onto the PCB at the location of the QFN package. Alternatively a stencil that applies the solder paste directly to the back of the QFN package can be used. Rework stencils are available from several manufacturers including the CPF (Component Print Frame) from Mini Micro Stencil Inc¹ (figure 6).

Solder Reflow can be accomplished using the hot-air workstation with care taken not to overheat the QFN package. Due to the small mass of the package, when the solder paste at the leads reflows, the bottom of the package will also reflow and the heat can then be removed.

Conclusion

The PCB layout, handling and assembly processes necessary to successfully integrate QFN packages into a system design have been detailed. These processes are easily integrated into standard PCB manufacturing lines. All of the layout and stencil drawings presented are available from the factory and can be obtained by contacting Hittite Microwave Corporation by phone or by going on-line at www.hittite.com and completing an inquiry form.

¹ www.minimicrostencil.com. For the LP3 package use part number CPF-16. For the LP4 package use part number CPF-24.

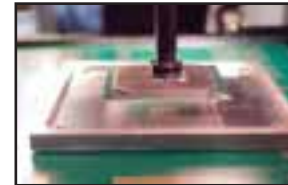


Figure 6 – Rework
CPF stencil